DOCUMENT NUMBER AND REVISION

VL-FS-MGLS12032C-01 REV. A

(MGLS12032C-LED04)

DOCUMENT TITLE:

SPECIFICATION

OF

LCD MODULE TYPE

CUSTOMER	
MODEL NUMBER	**MGLS12032C-01**
CUSTOMER APPROVAL	
DATE	

DEPARTMENT	NAME	SIGNATURE	DATE
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VARITRONIX LIMITED

Specification
of
LCD Module Type
Item No.: MGLS12032C-01

1. General Description

- 120 x 32 dots STN Positive Yellow Transflective Dot Matrix LCD Graphic Module.
- Viewing Angle: 6 O'clock direction.
- Driving scheme: 1/32 multiplexed drive, 1/6.7 bias.
- 'Epson' SED1520 D0A (Die form) dot matrix LCD drivers or equivalent.
- Yellow-green LED04 backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	84.0(W) x 44.0(H) x 14.0(D) MAX.	mm
Effective viewing area	61.0(W) x 15.8(H)	mm
Display format	120(H) x 32 (V)	dots
Dot size	0.43(W) x 0.39(H)	mm
Dot spacing	0.04(W) x 0.04(H)	mm
Dot pitch for characters	0.47(W) x 0.43(H)	mm
Weight:	TBD	grams

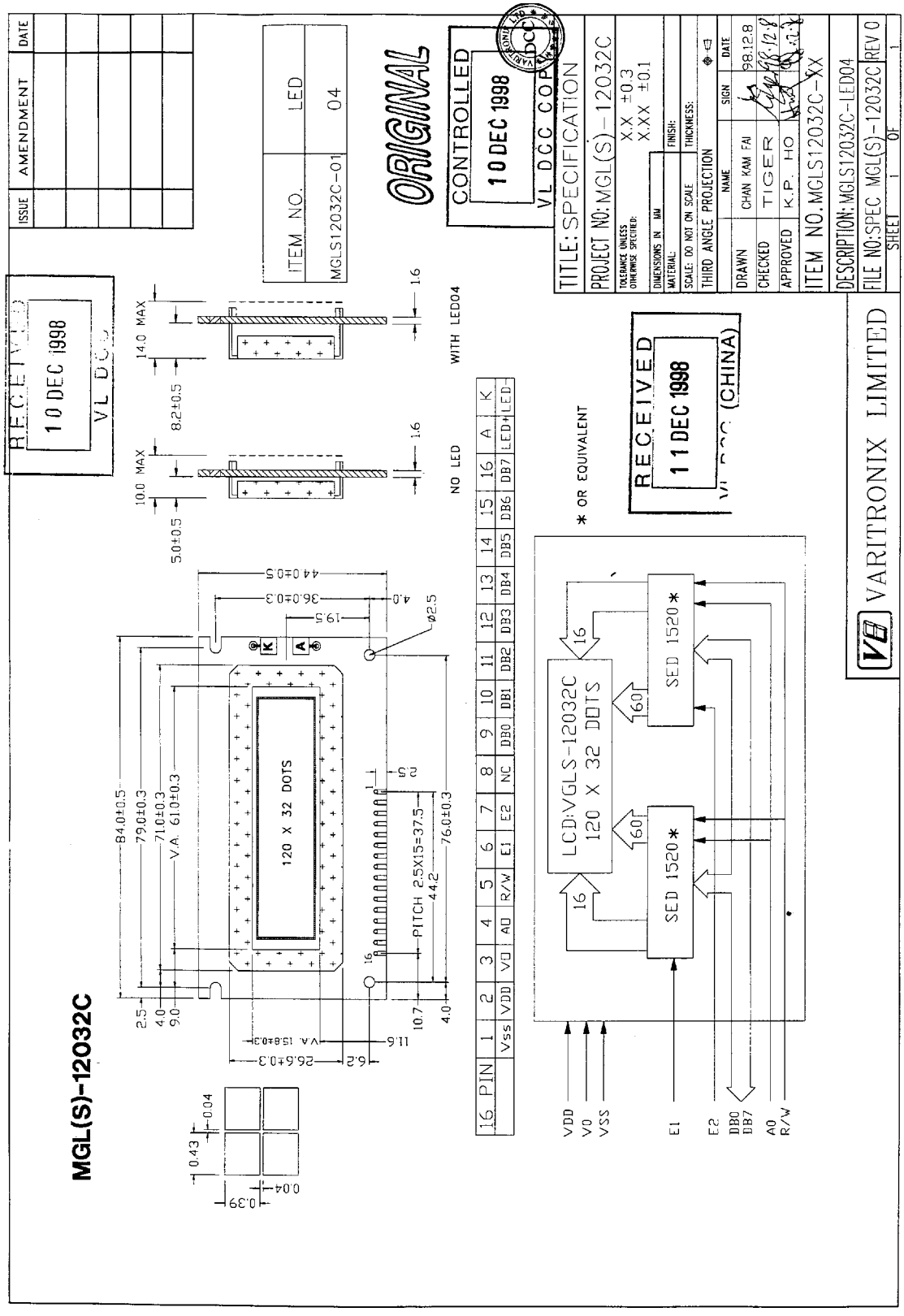

Figure 1: Specification Drawing

3. Interface signals

Table 2

Pin No.	Symbol	Description
1	VSS	Ground(0V)
2	VDD	Power supply for logic (+5V)
3	V0	Power supply for LCD driver
4	A0	Data/Command Select Input 'High': Display data on DB0-DB7. 'Low' : Display control data on DB0-DB7.
5	R/W	Chip interface with 68 family MPU: Read/Write control signal input pin. R/W = "High": Read control signals. R/W = "Low": Write control signals.
6	E1	For first LCD driver SED1520: Chip interfaced with 68 family MPU: Input. Active high. Enable clock signal input for the 68 family MPU.
7	E2	For second LCD driver SED1520: Chip interfaced with 68 family MPU: Input. Active high. Enable clock signal input for the 68 family MPU.
8	NC	No connection.
9	DB0	Data input/output (LSB)
10	DB1	Data input/output
11	DB2	Data input/output
12	DB3	Data input/output
13	DB4	Data input/output
14	DB5	Data input/output
15	DB6	Data input/output
16	DB7	Data input/output (MSB)
A	LED+	Anode of LED backlight.
K	LED-	Cathode of LED backlight.

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings(Ta = 25 ºC)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD - VSS	-0.3	+8.0	V
Power Supply voltage (LCD drive)	VLCD =VDD – V0	-0.3	+16.5	V
Input voltage	Vin	-0.3	VDD +0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 5V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD -VSS		4.75	5.0	5.25	V
Supply voltage (LCD)	VLCD =VDD –V0	VDD = 5V, Note 1.	8.8	9.3	9.8	V
Input signal voltage 1 for E,DB0-DB7,R/W,A0	V_{IH1}	”H” level	2.0	-	VDD	V
	V_{IL1}	” L” level	0	-	0.8	V
Supply current (Logic & LCD)	IDD	All mode	-	1.5	2.3	mA
Supply current (LCD)	I0	All mode, Note 1	-	1.4	2.1	mA
Supply voltage of yellow-green LED04 backlight	VLED	Forward current =90mA Number of LED dies =18.	3.9	4.1	4.3	V

Note (1) : There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

At Ta = 0°C to +50°C, VDD = 5V±5% ,VSS = 0V.
Refer to Fig. 2, MPU bus read / write timing diagram (68 family MPU)

Table 6

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
System Cycle Time	A0,/CS,R/W	t_{CYC6}	-	1000	-	ns
Address Set-up Time	A0,/CS,R/W	t_{AW6}	-	20	-	ns
Address Hold Time	A0,/CS,R/W	t_{AH6}	-	10	-	ns
Data Set-up Time	DB0-DB7	t_{DS6}	-	80	-	ns
Data Hold Time	DB0-DB7	t_{DH6}	-	10	-	ns
Output Disable Time	DB0-DB7	t_{OH6}	CL=100pF	10	60	ns
Access Time	DB0-DB7	t_{ACC6}	CL=100pF	-	90	ns
Enable Pulse Width(Read)	E	t_{EW}	-	100	-	ns
Enable Pulse Width(Write)	E	t_{EW}	-	80	-	ns
Rise & Fall Time	-	tr, tf	-	-	15	ns

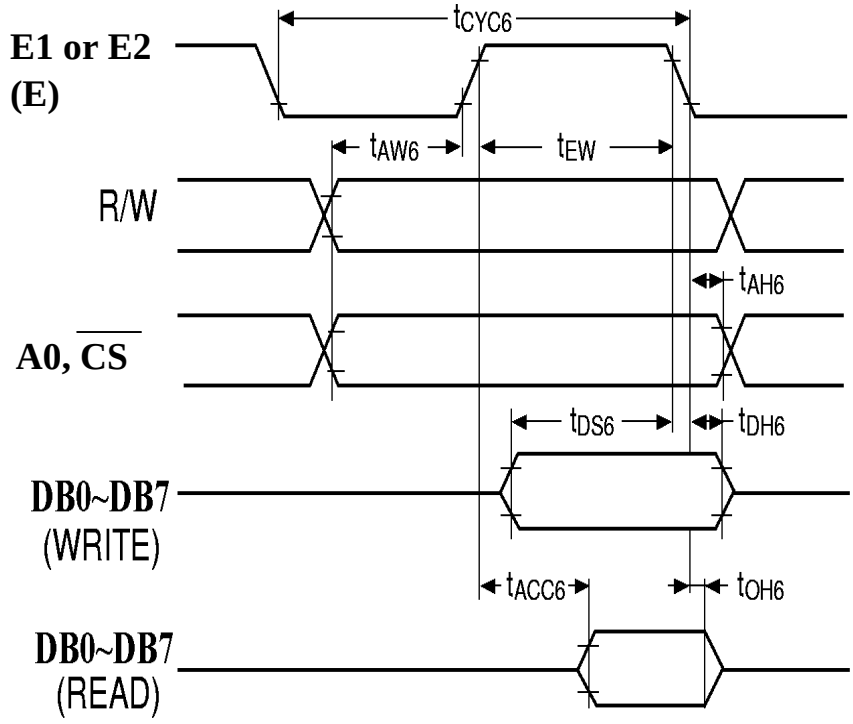

Figure 2: MPU bus read / write timing diagram (68 family MPU)

5.3 Timing Diagram of VDD against V0.

Power on sequence shall meet the requirement of Figure 3, the timing diagram of VDD against V0.

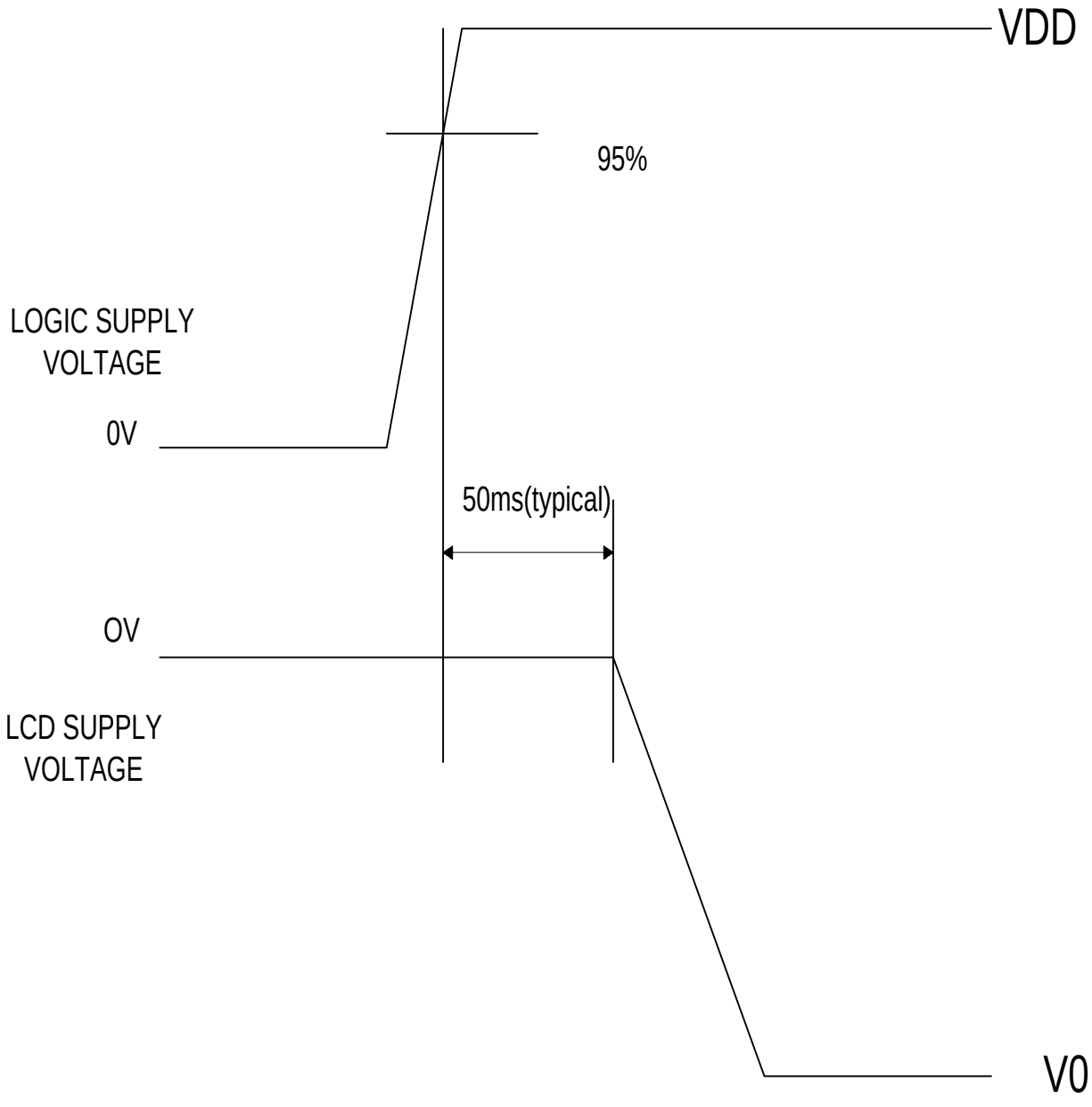

Figure 3: Timing diagram of VDD against V0.

"Varitronix Limited reserves the right to change this specification."

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